REMARKS

Entry of the foregoing, reexamination and reconsideration of the subject matter identified in caption, as amended, pursuant to and consistent with 37 C.F.R. §1.112, and light of the remarks which follow are respectfully requested.

Claims 1-29 are pending in the application. Of these, claims 1-12 have been withdrawn from consideration.

By the foregoing amendments, the claim 1 has been corrected to depend from claim 13. Claim 1 has also been revised by replacing "optical element" with "optical component" for consistency with other claims. Claim 21 has been amended to include patterned metal pad and solder features. Other amendments are for readability.

Turning now to the Official Action, claims 13-29 stand rejected under 35 U.S.C. §112, first paragraph. This rejection is respectfully traversed for the following reasons.

The Official Action states that it is not clear from where in the application support is drawn for the previously presented claim amendments relating to the dielectric layer being planar. Support can be found at least in Figure 1 taken with any of Figures 2-9 and the specification at page 9, lines 23-24. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 13-29 stand rejected under 35 U .S.C. §102(b) as being anticipated by *Ayliffe et al* (U.S. Patent No. 5,522,000). Claims 13-29 also stand rejected under 35 U.S.C. §103(a) as being obvious over *Ayliffe et al*. These rejections are respectfully traversed for the following reasons.

The present invention relates to etched optoelectronic apparatuses. The apparatuses as set forth, for example, in independent claim 13 comprises: a) a semiconductor substrate having an etched pit with semiconductor sidewalls; b) a dielectric layer disposed on the semiconductor substrate, wherein the dielectric layer is planar and has a hole with dielectric sidewalls, wherein the dielectric sidewalls are aligned with the semiconductor sidewalls; c) a patterned metal layer disposed directly on the dielectric layer, wherein the patterned metal layer has sidewalls aligned with the dielectric sidewalls and semiconductor sidewalls; and d) an optical element in the etched pit.

Ayliffe et al discloses a method of making a multilayered printed circuit on a single crystal substrate for mounting thereon at least one electro-optic transducer and at least one optical component. The printed circuit has a plurality of electrical conductors. (Col. 2, lines 1-5).

Ayliffe et al does not disclose or suggest each feature of the present invention. For example, *Ayliffe et al* does not disclose or fairly suggest an etched optoelectronic apparatus having a dielectric layer disposed on a semiconductor substrate, wherein the dielectric layer is planar, as set forth in independent claims 13, 24 and 27. Quite to the contrary, the metal pads 16b of *Ayliffe et al* sit directly on a dielectric layer 14 which is non-planar. In this regard, *Ayliffe et al* discloses that prior to depositing the dielectric layer 14, a passivation layer 11 is deposited, a patterned interconnect layer 13 is formed on layer 11 and a dielectric layer 14 is formed over the patterned interconnect layer 13. In this regard, *Ayliffe et al* discloses that:

> The next layer of the structure is a patterned interconnect layer 13 disposed on the passivation layer 11. Patterning is achieved by photolithography. . . . After removal of the metal-coated patterned lift-off layer, the patterned interconnect layer 13 is covered with a dielectric layer 14 which may comprise a thin silicon nitride passivation layer covered by a thicker layer of silica. Such material may conveniently be deposited by plasma enhanced chemical vapour deposition. (Col. 3, lines 29-46).

Persons skilled in the art know that PECVD-deposited layers such as described by *Ayliffe et al*, when deposited over a patterned interconnect layer would not result in a planar structure. The *Ayliffe et al* dielectric layer 14 formed over the patterned interconnect layer 13 would, in fact, be non-planar. *Ayliffe et al* requires formation of the interconnect layer 13, and there is no disclosure or suggestion in that document to form anything other than a multilayered printed circuit having such a structure. Thus, the present invention is not disclosed by *Ayliffe et al*, and persons skilled in the art would not have modified the *Ayliffe et al* multilayered printed circuit to arrive at applicants' invention. Accordingly, withdrawal of these rejections is respectfully requested.

As a final matter, it is noted that newly presented claim 30 is not disclosed or suggested by *Ayliffe et al* at least because that document does not disclose or suggest a

metal pad structure comprising a first region for receiving an active optoelectronic device and a second region for electrical connection, wherein the patterned metal layer is formed form a single mask. In this regard, the *Ayliffe et al* pad 16a and patterned interconnect layer 13 is not formed from a single mask.

From the foregoing, further and favorable action in the form of a Notice of Allowance is believed to be next in order, and such action is earnestly solicited.

If there are any questions concerning this paper or the application in general, the Examiner is invited to telephone the undersigned at his earliest convenience.

Respectfully submitted,

Jonathan D. Baskin
Attorney for Applicant
Registration No. 39,499
Telephone No.: (508) 787-4766
Facsimile No.: (508) 787-4730

c/o EDWARDS & ANGELL, LLP
P.O. Box 9169
Boston, Massachusetts 02209
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